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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BARRECA, NICOLE M	

ART UNIT	PAPER NUMBER
1756	10

DATE MAILED: 10/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,760	IRELAND ET AL.	
	Examiner	Art Unit	
	Nicole M. Barreca	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32,34-51 and 55-62* is/are pending in the application.

4a) Of the above claim(s) *55-57* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32,34-51 and 58-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 32, 34-51, and 55-62 are pending in this application. Claims 55-57 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 7.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

3. The use of the trademarks DARC1 and DARC2 have been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology. While the trademarks are capitalized in the specification, they should also be accompanied by generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 32, 34-38, 58, 59, 61, 62 are rejected under 35 U.S.C. 102(e) as being anticipated by Blatchford (US6200734).

6. Blatchford discloses a method for fabricating semiconductor devices in integrated circuits using photolithography. The semiconductor device comprises substrate 10, field oxides 11 of varying topography, metal layer 18 (reflective), antireflection coating 17 and photoresist layer 16. The layer of metal will ultimately be patterned to gate electrodes when the MOSFET device is formed. The antireflection coating 17 comprises three layers 13-15 of silicon containing oxide, each with different indices of refraction (n) and extinction coefficients or absorptions (k). The antireflection layers are used to eliminate the interference patterns caused by the rays reflected by the underlying topography when the photoresist is exposed (col.1, 18-col.2, 64). When there are three antireflection layers, the first antireflection layer 13 is formed with a thickness of 350-450 angstroms (35-45 nm), while the second antireflection layer 15 is formed with a thickness between 150-250 angstroms (15-25 nm). For the first antireflection layer, k1 is between about 1.1-1.9 and for the second antireflection layer, k2 is between about 0.15-0.3. The index of refraction n2 is in the range of 1.7-2.0 (col.4, 49-61). In order to prevent crosslinking between the photoresist layer 16 and the antireflection coating 17, an additional oxynitride layer 19 (dielectric material, cl.37) is formed there between (col.3, 8-15).

7. Claims 32, 34, 60-62 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohta (US 6268295).

8. Ohta teaches a method for making a semiconductor device. Figure 10A teaches a gate electrode 34 (reflective surface) over which a first SiO2 film 40, a first antireflective film 42, a second antireflective film 45 and a third SiO2 film 46 (applicant's second silicon dioxide layer) are formed (col.10, 12-56).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford.

11. Blatchford teaches that k1 is between about 1.1-1.9, k2 is between about 0.15-0.3 and n2 is in the range of 1.7-2.0 (col.4, 49-61). Blatchford also teaches that the indices of refraction for the antireflective layers are different, but is silent on the specific index of refraction for the first antireflective layer, n1, (for the embodiment where there are three antireflective layers), and does not disclose that the first index of refraction is approximately 2.1. However Blatchford teaches that the indices of refraction are varied in the three layers by varying the ratio of silane to nitrous oxide during the deposition and are designed to with used with a photoresist layer which is exposed to DUV light in order to avoid destructive interference of the reflected rays, thereby establishing the

indices of refraction as result-effective variables. It would have been within the ordinary skill of one in the art to determine the optimal index of refraction for the first antireflection layer in Blatchford by routine experimentation and to have the thickness be approximately 2.1, if required, because Blatchford establishes that the index of refraction is a result-effect variable and the discovery of an optimum value of a result effective variable is ordinary within the skill of the art (*In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980)).

12. Claims 40-45, 47-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford in view of Fukuda (US 6255151).

13. The teachings of Blatchford have been discussed above. Blatchford teaches a structure comprising three antireflection layers having different indices of refraction, a dielectric layer and a photoresist layer for patterning use in the manufacture of a semiconductor device. Blatchford however is silent on the specific semiconductor device being formed and does not disclose that the semiconductor device comprises a memory cell comprising at least two active areas, a gate stack between the active areas, and a capacitor in electrical contact with one of the active areas (cl.40), or that the structure is a DRAM cell comprising first, second and third active areas, first and second gate stacks and first and second capacitors, the first gate stack being formed between the first and second active areas, the second gate stack being formed between the second and third active areas, the first capacitor being in electrical contact with the first active area, the second capacitor being in electrical contact with the third active area, and the second active area being in electrical contact with a bit line (cl.44), or that

the capacitors are formed over the gate stacks (cl.45), or that the bit line is formed over the capacitors (cl.47).

Fukuda teaches that memory cells of a DRAM are generally placed at points where a plurality of word and bit lines intersect on a principal surface of the semiconductor substrate in matrix form. Each memory cell comprises one memory cell section (MISFET) and one capacitor electrically connected in series therewith. The memory cell selection is formed within an active region, is surrounded by a device separation region and comprises a gate oxide, a gate electrode constructed with each word line, and a source/drain pair. Each bit line is placed at an upper portion of the memory cell and is electrically connected to one of the source and drain shared by two adjacent memory cells, while the capacitor is also placed in the upper portion and electrically connected to the other of the source and drain (col.1, 14-33). It would have been obvious to one of ordinary skill in the art to have the structure comprising the semiconductor substrate, three antireflection layers, dielectric layer and photoresist layer in Blatchford to additionally include components such as active regions, gate stacks, capacitors and bit lines, arranged as claimed (cl.40, 45, 47), because Fukada teaches that such components in this arrangement are conventional for a memory cell in the art. While Fukuda does not explicitly disclose that there are three active regions that are specifically arranged as claimed in cl.44, the reference does teach that there are a plurality of memory cells and bit and word lines, arranged in series. It would have been within the ordinary skill of one in the art to determine the exact number of active

regions and cells required for the specific device being manufactured because Fukuda teaches that such memory cells and their general structure are known in the art.

With respect to claim 49, Blatchford teaches that k1 is between about 1.1-1.9, k2 is between about 0.15-0.3 and n2 is in the range of 1.7-2.0 (col.4, 49-61). Blatchford also teaches that the indices of refraction for the antireflective layers are different, but is silent on the specific index of refraction for the first antireflective layer (for the embodiment where there are three antireflective layers), and does not disclose that the first index of refraction is approximately 2.1. However Blatchford teaches that the indices of refraction are varied in the three layers by varying the ratio of silane to nitrous oxide during the deposition and are designed to with used with a photoresist layer which is exposed to DUV light in order to avoid destructive interference of the reflected rays, thereby establishing the indices of refraction as result-effective variables. It would have been within the ordinary skill of one in the art to determine the optimal index of refraction for the first antireflection layer in Blatchford by routine experimentation and to have the thickness be approximately 2.1, if required, because Blatchford establishes that the index of refraction is a result-effect variable and the discovery of an optimum value of a result effective variable is ordinary within the skill of the art (*In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980)).

14. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford in view of Fukuda as applied to claim 45 above, and further in view of Chen (US 6140179).

15. While Blatchford in view of Fukuda teaches capacitors arranged in the memory cell, the references do not disclose that the capacitors are container capacitors. Chen teaches that crown (or container) capacitors conventional in the art (col.2, 23-27, col.3, 5-6). It would have been obvious to one of ordinary skill in the art to have the capacitor in Blatchford in view of Fukuda be a container capacitor because Chen teaches crown (container) capacitors are conventional in the art.

16. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford in view of Kim (US 6258691) and Fukuda.

17. The teachings of Blatchford have been discussed above. Blatchford teaches a structure comprising three antireflection layers having different indices of refraction, a dielectric layer and a photoresist layer for patterning use in the manufacture of a semiconductor device. Blatchford does not disclose that the (insulating) antireflective layers are an etch stop layer. Kim teaches a method for making a capacitor wherein antireflective layers are also used as an etch stop layer (col.11, 36-37). It would have been obvious to one of ordinary skill in the art to have the antireflective layers in Blatchford to be used as an etch stop layer because Kim teaches a method for making a capacitor wherein antireflective layers are also used as an etch stop layer.

Blatchford is silent on the specific semiconductor device being formed and does not disclose that the semiconductor device comprises a memory cell comprising at least two active areas, a gate stack between the active areas, and a capacitor in electrical contact with one of the active areas. Fukuda teaches that memory cells of a DRAM are generally placed at points where a plurality of word and bit lines intersect on a principal

surface of the semiconductor substrate in matrix form. Each memory cell comprises one memory cell section (MISFET) and one capacitor electrically connected in series therewith. The memory cell selection is formed within an active region, is surrounded by a device separation region and comprises a gate oxide, a gate electrode constructed with each word line, and a source/drain pair. Each bit line is placed at an upper portion of the memory cell and is electrically connected to one of the source and drain shared by two adjacent memory cells, while the capacitor is also placed in the upper portion and electrically connected to the other of the source and drain (col.1, 14-33). It would have been obvious to one of ordinary skill in the art to have the structure comprising the semiconductor substrate, antireflection layers, dielectric layer and photoresist layer in Blatchford in view of Kim to additionally include components such as active regions, gate stacks, capacitors and bit lines, arranged as claimed in claim 50 because Fukada teaches that such components in this arrangement are conventional for a memory cell in the art.

18. Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford in view of Fukada and Podlesny (US 5724299).

19. The teachings of Blatchford and Fukuda have been discussed above. Blatchford teaches a structure comprising three antireflection layers having different indices of refraction, a dielectric layer and a photoresist layer for use in the manufacture of a semiconductor device, while Fukuda teaches the components and arrangement of a conventional memory cell. The references however do not disclose a computer system comprising a processor and a memory comprising at one memory cell comprising the

components as claimed. Podlesny teaches that a memory cell array is typically used as memory for a computer system having a processor (col.6, 42-46). It would have been obvious to one of ordinary skill in the art to have the memory cell including the multiple antireflective layers in Blatchford in view of Fukuda as the memory, along with a processor, in order to form a computer system because Podlesny teaches that it is known in the art to use a memory cell array as memory for a computer system having a processor.

Response to Arguments

20. The rejection using the Figura reference has been withdrawn in response to the applicant's statement regarding common ownership. A new rejection was applied to claim 46. Applicant's arguments with respect to claim 50 have been considered but are moot in view of the new ground(s) of rejection.

21. Applicant's arguments filed 8/6/03 have been fully considered but they are not persuasive. With respect to claim 32, the applicant argues that Blatchford does not teach that the reflected radiation cancels. However Blatchford does teach that the antireflection layers are used to eliminate the interference patterns caused by the rays reflected by the underlying topography when the photoresist is exposed (col.1, 18-col.2, 64). In addition that limitations and the limitation reciting how the indices of refraction, absorptions and thicknesses are chosen are process limitations which do not further limit the product claims. With respect to claims 40 and 51 the applicant argues that the references do not teach that the antireflective coating is adapted to stop an etch

process. However this limitation is a process limitation which does not further limit the product claims.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nicole M. Barreca whose telephone number is 703-308-7968. The examiner can normally be reached on Monday-Thursday (8:00 am-6: 30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 703-308-2464. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

Nicole Barreca
Patent Examiner
Art Unit 1756
10/20/03